AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings of claims in this application.

1. (Currently Amended) A method of writing to cache comprising:

initiating a write operation to a cache;

in a first operational mode:

detecting the presence or absence of a write miss;

if a write miss is absent, writing data to said cache;

if a write miss is present, retrieving said data from a further memory and writing said data to said cache;

in a second operational mode:

placing said cache in a memory mode for performing a cache write;

writing said data to said cache regardless of whether a write miss is present or absent to update a cache directory with the contents of a target address.

2. (Original) The method of claim 1 wherein:

said second operational mode is designated by a memory mode bit.

3. (Original) The method of claim 2 wherein:

said memory mode bit is stored in a device control register.

4. (Original) The method of claim 1 wherein:

said initiating a write operation includes specifying an address;

said second operational mode is designated by address bits contained within said address.

5. (Original) The method of claim 4 wherein:

said by address bits contained within said address include the high order address bits equaling 1111.

6. (Original) The method of claim 1 wherein:

said initiating a write operation includes specifying an address;

said second operational mode includes retrieving a bin identifier from said address, said bin identifier designating a compartment of said cache where said data is to be written.

7. (Original) The method of claim 1 wherein:

said second operational mode includes setting a select all bins bit to invalidates cache directory entries associated with writing said data.

8. (Currently Amended) A system of writing to cache comprising:

a cache directory;

a cache array;

control logic for writing a valid field and an address to said cache directory and data to said cache array, said control logic including:

hit miss complex logic for determining a compartment of said cache directory and said cache array to be updated upon detecting a cache hit in a first operation mode;

least recently used (LRU) complex logic for determining a compartment of said cache directory and said cache array to be updated upon detecting a cache miss in said first operational mode;

said control logic determining a compartment of said cache directory and said cache array to be updated regardless of a cache hit or cache miss in a second operational

mode for performing a cache write to update the cache directory with the contents of a target address.

9. (Original) The system of claim 8 wherein:

said second operational mode is designated by a memory mode bit.

10. (Original) The system of claim 9 further comprising:

a device control register storing said memory mode bit.

11. (Original) The system of claim 8 wherein:

said second operational mode is designated by address bits contained within said address.

12. (Currently Amended) The system of claim 11 wherein:

said ~~by~~ address bits contained within said address include the high order address bits equaling 1111.

13. (Original) The system of claim 8 wherein:

said control logic retrieves a bin identifier from said address, said bin identifier designating said compartment of said cache where said data is to be written.

14. (Original) The system of claim 8 wherein:

said control logic invalidates cache directory entries associated with writing said data in response to a select all bins bit.